PRODUCT SPECIFICATION

J102H-RR

Wi-Fi Single-band 1x1 802.11b/g/n + BLE5.0

Combo Module

Version:V5.0

Customer: ______________________________

Customer P/N:___________________________

Signature:______________________________

Date:__________________________________

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J102H-RR Module Datasheet

Ordering Information	Part NO.	Description
	FGJ102HRRX-00	BL602C-00-Q2I,b/g/n Wi-Fi/BLE 1T1R,18x20mm，板载天线

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Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2021/03/16	New version	Fc	Zzq	Qjp
V2.0	2021/04/21	Pin define Modify	Fc	Zzq	Qjp
V3.0	2022/10/26	Dimensional drawing modification	Fc	Zzq	Qjp
V4.0	2022/12/16	Update braid direction	Fc	Zzq	Qjp
V5.0	2023/08/02	Modify the frequency range Modify the frequency band Modify Output Power Increase the antenna clearance area	Lxp	Zzq	Qjp

1. General Description

1.1 Introduction

J102H-RR is a Wi Fi + ble combination chipset for low-power and high-performance application development. The wireless subsystem includes 2.4G radio, Wi Fi 802.11b/g/n and ble 5.0 baseband / MAC design. The microcontroller subsystem contains a low-power 32-bit RISC CPU, cache and memory. In addition, various security features are supported.

1.2 Description

Model Name	J102H-RR
Product Description	Support Wi-Fi/BLE functionalities
Dimension	L x W x H: 18 x 20 x 3.05 mm
Wi-Fi Interface	Support UART
BT Interface	UART
Operating temperature	-20°C to 85°C
Storage temperature	-40°C to 125°C

2. Features

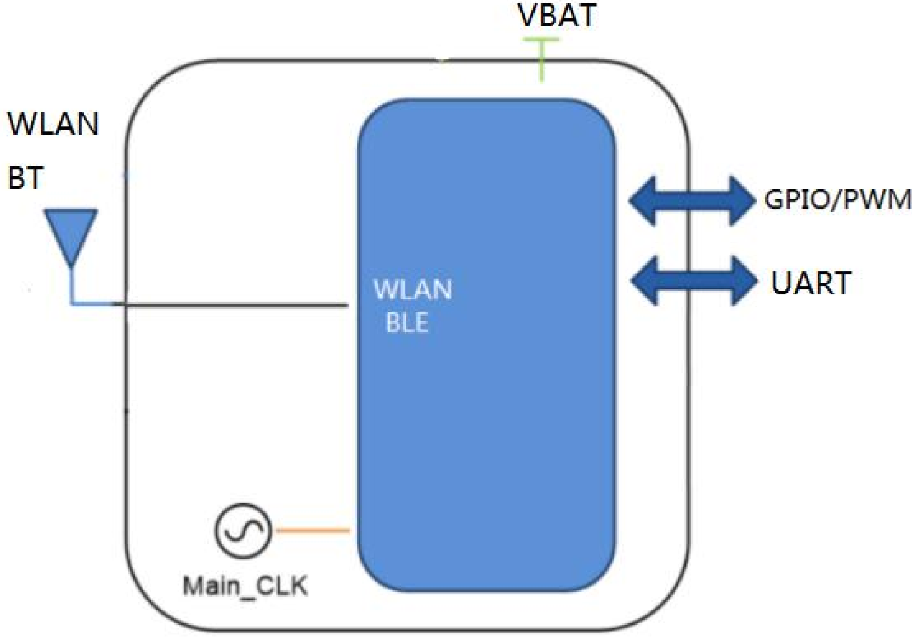
General Features

- Support IEEE 802.11 b/g/n agreement
- 2.4 GHz band 1t1r mode, support 20 MHz, data rate up to 72.2 Mbps
- Wi-Fi security WPS/WEP/WPA/WPA2 Personal/WPA2Enterprise/WPA3
- It supports station + ble mode and station + SoftAP + ble mode
- Coexistence of Wi Fi and ble

WLAN Interface

- Bluetooth low energy consumption 5.0，Bluetooth Mesh
- Ble helps achieve Wi Fi fast connection
- Support ble 5.0 channel selection 2

3. Block Diagram



4. General Specification

4.1 2.4G RF Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11 b/g/n/ Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 18dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
Test Items	**TYP Test Value**	**Standard Value**
Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps @ -92 dBm	≤-83 dBm
	- 11Mbps @ -85 dBm	≤-76 dBm
Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps @ -89 dBm	≤-85 dBm
	- 54Mbps @ -70 dBm	≤-68 dBm
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 @ -89 dBm	≤-85 dBm
	- MCS=7 @ -68 dBm	≤-67 dBm
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	

4.2 Bluetooth Specification

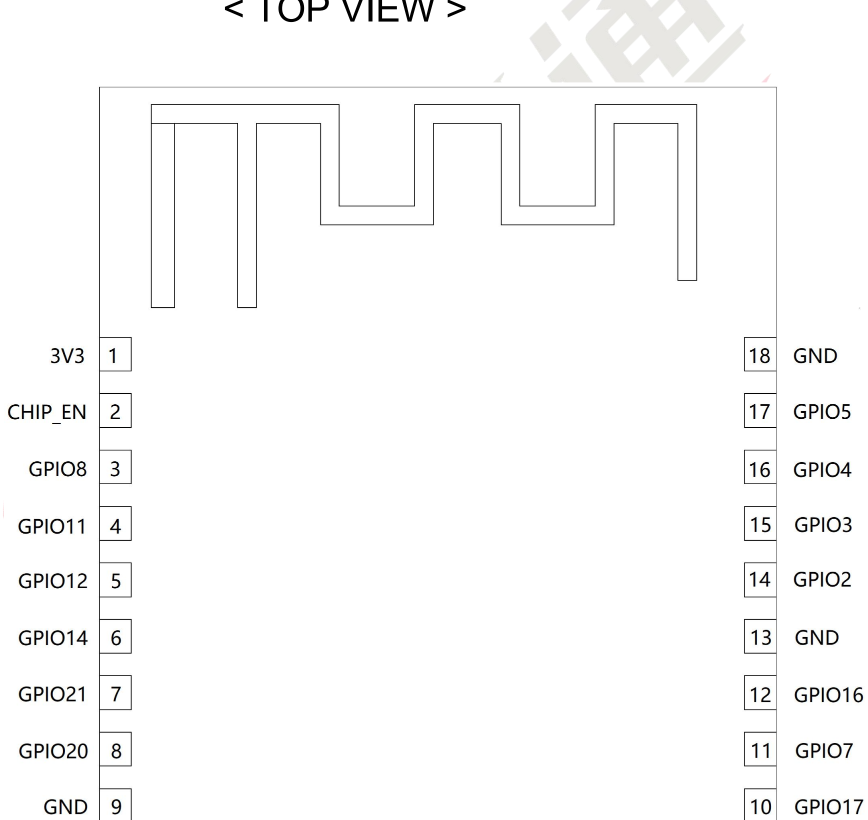
Feature	**Description**
General Specification	
Bluetooth Standard	Bluetooth V5.0
Host Interface	UART
Frequency Band	2400 MHz ~ 2483.5 MHz
Number of Channels	40 channels
RF Specification	

	Min(dBm)	**Typical**(dBm)	**Max**(dBm)
Output Power (Class 1)	2	5	8
Sensitivity @ BER=0.1% for GFSK (1Mbps)			-70
Maximum Input Level	GFSK (1Mbps):-20dBm		

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	3V3	P	3.3V	
2	CHIP_EN	I	Power enable of module ON: pull high ; OFF: pull low Pin Function Table	

3	GPIO8	I/O	Boot strap selection.Pin state sampled on rising edge of CHIP_EN. High: Boot from interface. Low: Boot from flash.	
4	GPIO11	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
5	GPIO12	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
6	GPIO14	I/O	GPIO Pin.　Chip Jtag TDO pin，Not recommended	
7	GPIO21	I/O	Connect to FLASH and do not use	VDDIO
8	GPIO20	I/O	Connect to FLASH and do not use	3.3V
9	GND	P	Ground connections	
10	GPIO17	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
11	GPIO7	I/O	GPIO Pin/UART RX	VDDIO
12	GPIO16	I/O	GPIO Pin/UART TX	VDDIO
13	GND	P	Ground connections	VDDIO
14	GPIO2	I/O	Connect to FLASH and do not use	VDDIO
15	GPIO3	I	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
16	GPIO4	O	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
17	GPIO5	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
18	GND	P	Ground connections	

P:POWER　I:INPUT　O:OUTPUT　VDDIO: 3.3V

download：3.3V，GPIO7,GPIO16,GND,,GPIO8 is pulled up before the module is powered on.

RF test：3.3V，GPIO7,GPIO16,GND,GPIO8 is suspended or pulled down.

5.3 Pin function group table

Pin Name	Flash[1]	SDIO	SPI (Default /SWAP=1)	UART[2](Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	IR
PAD_GPIO_0	SF2_D1	CLK	MOSI /MISO	SIG0 /SIG4	SCL	PWM_CH0	-	FEM0	TMS/TCK	-
PAD_GPIO_1	SF2_D2	CMD	MISO /MOSI	SIG1 /SIG5	SDA	PWM_CH1	-	FEM1	TDI/TDO	-
PAD_GPIO_2	SF2_D3	DAT0	SS	SIG2 /SIG6	SCL	PWM_CH2	-	FEM2	TCK/TMS	-
PAD_GPIO_3	-	DAT1	SCLK	SIG3 /SIG7	SDA	PWM_CH3	-	FEM3	TDO/TDI	-
PAD_GPIO_4	-	DAT2	MOSI /MISO	SIG4 /SIG0	SCL	PWM_CH4	ADC_CH1	FEM0	TMS/TCK	-
PAD_GPIO_5	-	DAT3	MISO /MOSI	SIG5 /SIG1	SDA	PWM_CH0	ADC_CH4	FEM1	TDI/TDO	-
PAD_GPIO_6	-	-	SS	SIG6 /SIG2	SCL	PWM_CH1	ADC_CH5	FEM2	TCK/TMS	-
PAD_GPIO_7	-	-	SCLK	SIG7 /SIG3	SDA	PWM_CH2	-	FEM3	TDO/TDI	-
PAD_GPIO_8	-	-	MOSI /MISO	SIG0 /SIG4	SCL	PWM_CH3	-	FEM0	TMS/TCK	-
PAD_GPIO_9	-	-	MISO /MOSI	SIG1 /SIG5	SDA	PWM_CH4	ADC_CH6/7	FEM1	TDI/TDO	-
PAD_GPIO_10	-	-	SS	SIG2 /SIG6	SCL	PWM_CH0	MICBIAS /ADC_CH8/9	FEM2	TCK/TMS	-
PAD_GPIO_11	-	-	SCLK	SIG3 /SIG7	SDA	PWM_CH1	ADC_CH10 /IRTX	FEM3	TDO/TDI	IRRX (ir_rx_gpio_sel=1)
PAD_GPIO_12	-	-	MOSI /MISO	SIG4 /SIG0	SCL	PWM_CH2	ADC_CH0	FEM0	TMS/TCK	IRRX (ir_rx_gpio_sel=2)
PAD_GPIO_13	-	-	MISO /MOSI	SIG5 /SIG1	SDA	PWM_CH3	ADC_CH3 /DAC_A	FEM1	TDI/TDO	IRRX (ir_rx_gpio_sel=3)
PAD_GPIO_14	-	-	SS	SIG6 /SIG2	SCL	PWM_CH4	ADC_CH2 /DAC_B	FEM2	TCK/TMS	-
PAD_GPIO_15	-	-	SCLK	SIG7 /SIG3	SDA	PWM_CH0	psw_irrcv_out /ADC_CH11	FEM3	TDO/TDI	-
PAD_GPIO_16	-	-	MOSI /MISO	SIG0 /SIG4	SCL	PWM_CH1	-	FEM0	TMS/TCK	-
PAD_GPIO_17	SF1_D3	-	MISO /MOSI	SIG1 /SIG5	SDA	PWM_CH2	-	FEM1	TDI/TDO	-
PAD_GPIO_18	SF1_D2	-	SS	SIG2 /SIG6	SCL	PWM_CH3	-	FEM2	TCK/TMS	-
PAD_GPIO_19	SF1_D1	-	SCLK	SIG3 /SIG7	SDA	PWM_CH4	-	FEM3	TDO/TDI	-

Pin Name	Flash[1]	SDIO	SPI (Default /SWAP=1)	UART[2](Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	IR
PAD_GPIO_20	SF1_D0 /SF2_D0	-	MOSI /MISO	SIG4 /SIG0	SCL	PWM_CH0	-	FEM0	TMS/TCK	-
PAD_GPIO_21	SF1_CS /SF2_CS	-	MISO /MOSI	SIG5 /SIG1	SDA	PWM_CH1	-	FEM1	TDI/TDO	-
PAD_GPIO_22	SF1_CLK /SF2_CLK	-	SS	SIG6 /SIG2	SCL	PWM_CH2	-	FEM2	TCK/TMS	-
PAD_GPIO_23	SF0_CLK	-	-	-	-	-	-	-	-	-
PAD_GPIO_24	SF0_CS	-	-	-	-	-	-	-	-	-
PAD_GPIO_25	SF0_D0	-	-	-	-	-	-	-	-	-
PAD_GPIO_26	SF0_D1	-	-	-	-	-	-	-	-	-
PAD_GPIO_27	SF0_D2	-	-	-	-	-	-	-	-	-
PAD_GPIO_28	SF0_D3	-	-	-	-	-	-	-	-	-

6. Electrical Specifications

6.1 Power Supply DC Characteristics

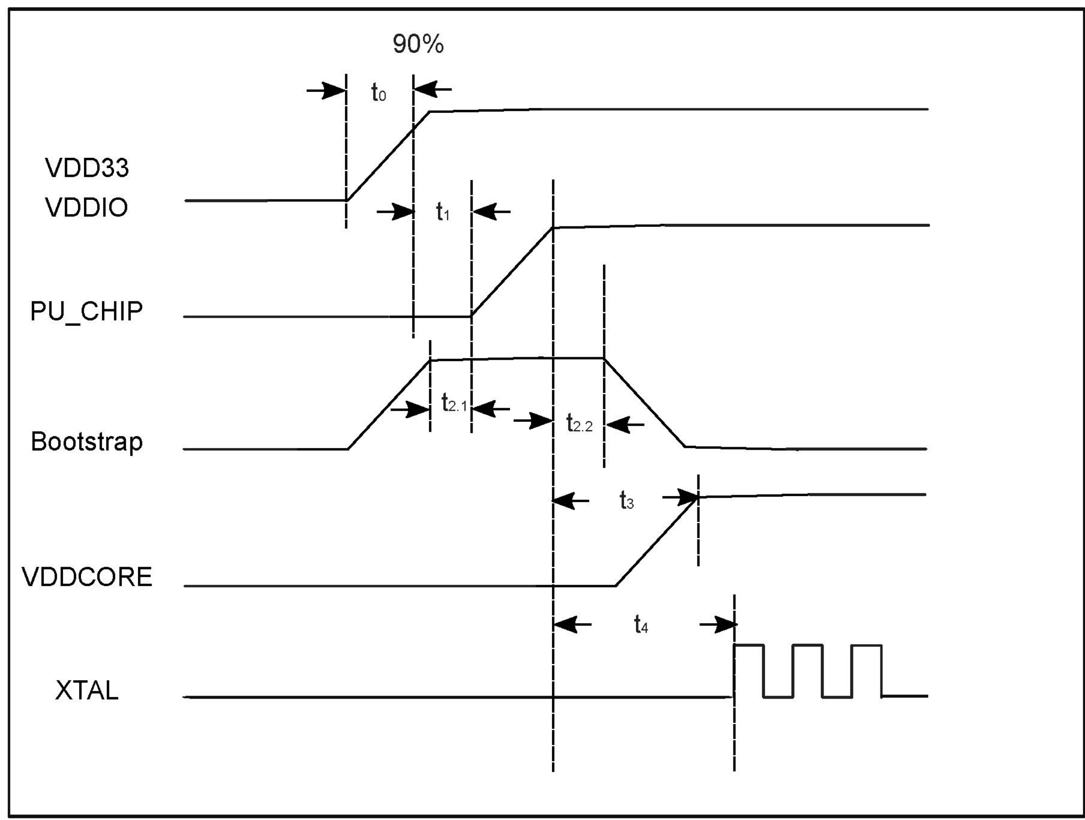
	MIN	TYP	MAX	Unit
Operating Temperature	-20	25	85	deg.C
VCC33	3.0	3.3	3. 6	V
VDDIO	3.0	3.3	3. 6	V

6.2 Power Consumption

Mode		Note	Performance @3.3Vdc 25◦C			
			Min.	Typ	Max.	Unit
RX	11b			35		mA
	11g			39		
	11n			39		
	BLE 1Mbps	Duty 60%		31		
TX	11b - 11Mbps @21dBm	Duty 50%		190		
		Duty 99%		310		
	11g - 54Mbps @18dBm	Duty 50%		145		
		Duty 99%		230		
	11n - MCS7 @17dBm	Duty 50%		130		
		Duty 99%		215		
	BLE 1Mbps @15dBm	Duty 86%		133		

6.3 Power-on sequence

In order to ensure normal power on and start, the power supply, reset and bootstrap pins need to meet the corresponding timing requirements.



paramete	explain	Min(ms)	Typical(ms)	Max(ms)
t_0	Rise time of power supply voltage reaching 90%			2
t_1	Power up to Pu_ Delay before chip pull-up	0.1		
$t_{2.1}$	Boostrap pin[1] Level at PU_ Setup time before chip is raised	0		
$t_{2.2}$	Boostrap Pin level in Pu_ Holding time after chip is pulled up	2		
t_3	PU_ Chip pulled up to vddcore output		2	
t_4	PU_ Chip is pulled up to XTAL for vibration		2	

[1] Bootstrap pin is GPIO8。

7. Size reference

7.1 Module Picture

L x W : 18 x 20 (+0.3/-0.1) mm	
H: 3.05 (±0.2) mm	3. 05
重量	TBD

7.2 Marking Description

公司Logo ----- Fn-Link
产品型号 ----- J102H-RR
生产批次 ----- CXXXXX
00代表机型 ----- 220300
Pin 1 标记
生产周期

7.3 Physical Dimensions

7.1

0.85

20

3.9

2.4

0.9

0.9

2.4

0.9

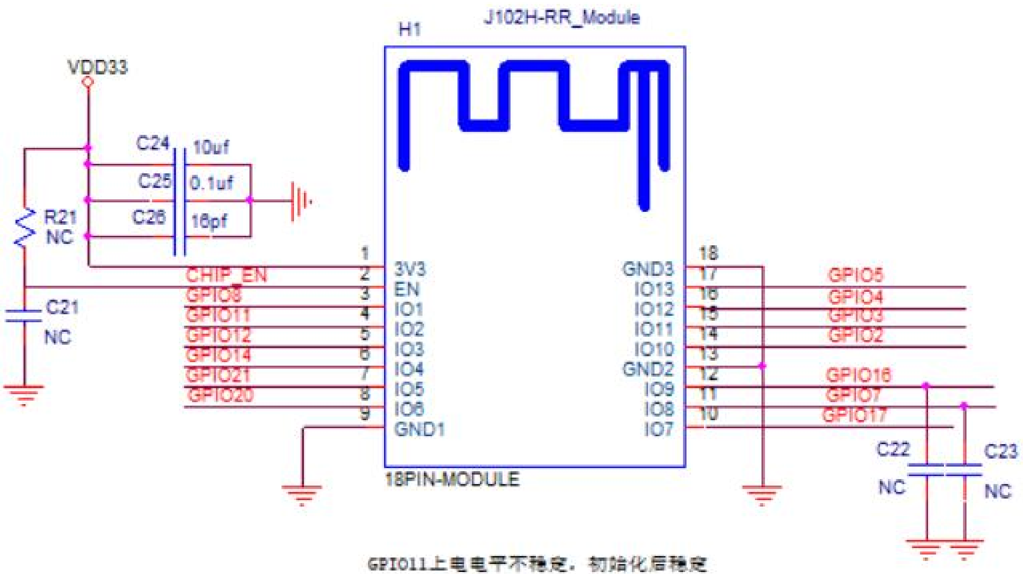
18

7.4 Layout Recommendation

8. The Key Material List

Item	Part Name	Description	Manufacturer
1	Crystal	3225 40MHz ±10ppm,12pF	ECEC, TKD, Hosonic, JWT, TXC
2	Chipset	BL602C-00-Q2I QFN32	博流
3	PCB	J102H-RR 4L,FR4,18*24mm	XY-PCB,GDKX,Sunlord, SL-PCB
4	Shielding	J102H-RR Shielding	信太，精力通

9. Reference Design



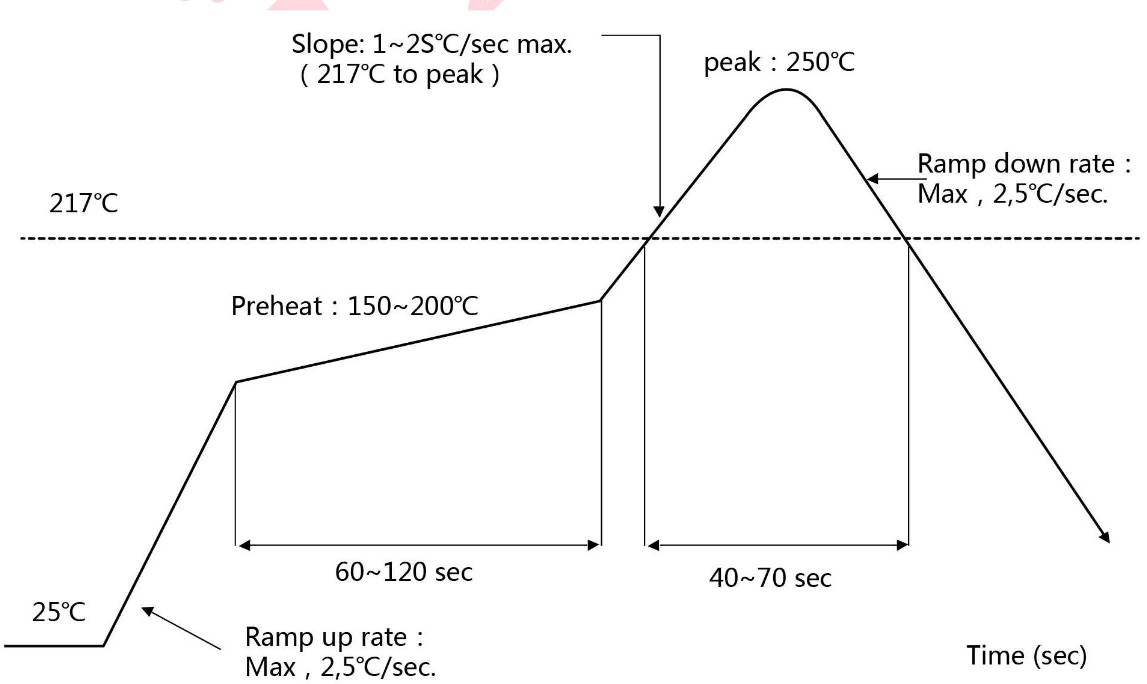
10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature: 250±5 °C

5Time within 5° C of peak temperature：≥10s

Number of Times: 2 times



11. Antenna clearance area requirements

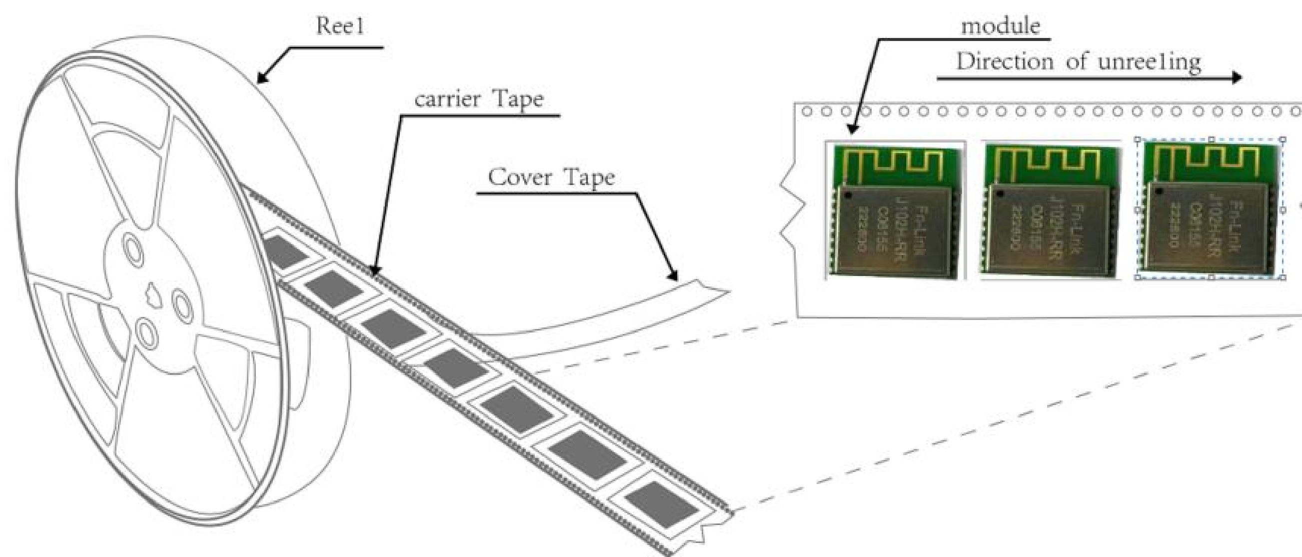
When using PCB antenna on Wi-Fi module, make sure the distance between PCB on motherboard and other metal devices is at least 16mm.The shaded areas in the figure below need to be marked away from metal devices, sensors, interference sources, and other materials that may interfere with the signal.

Figure 6-2 Antenna clearance reference

12. Package

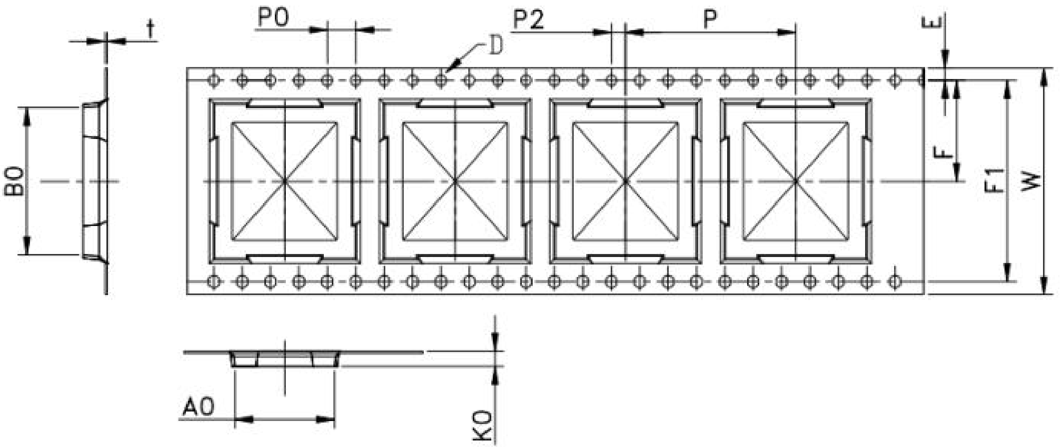
12.1 Reel

A roll of 800pcs



12.2 Carrier Tape Detail

ITEM	W	A0	B0	D	E	F	F1	K0	P0	P2	P	T
DIM	32	18.40	20.30	1.5	1.75	14.20	28.4	3.50	4.0	2.0	24.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	±0.1	±0.15	±0.10	±0.10	±0.1	±0.15	±0.1	±0.05

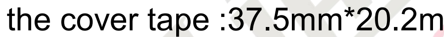


12.3 Packaging Detail

The take-up package:

Using self-adhesive tape

Size of black tape:44mm*20.2m



the cover tape :37.5mm*20.2m

Color of plastic disc: blue

NY bag size: 415mm*450mm

size ： 350X350X35mm

Carton size: 360X210X370mm

13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

d) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

e) Baking is required if conditions b) or c) are not respected

f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more